AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 20, line 23, and ending at page 30, line 8, with the following paragraph rewritten in amendment format:

Therefore, in the display device having the foregoing arrangement, the dot clock DCK, the horizontal synchronization signal Hsync and the vertical synchronization signal Vsync are oscillated when the driving control signal Scan is high level, and the dot clock DCK, the horizontal synchronization signal Hsync and the vertical synchronization signal Vsync are not oscillated when the driving control signal Scan is low level, as shown in ~~Figure 5~~ Figure 7; namely, the DCK-PLL circuit 6 and the medium-speed PLL circuit 10 and the inaction cycle oscillation circuit 12 are stopped.

On page 30, between lines 16 and 17, please insert the following paragraph:

Figure 7 is a drawing showing waveforms of a dot clock (DCK), a horizontal synchronization signal (Hsync), a vertical synchronization signal (Vsync) and a driving control signal (Scan) of the display device shown in Figure 6.